< DE/EJ/ET/EN/EX/EQ/IE/IS/IC >: <22636>: <Emerging Trends in Electronics>: <Advance Processors>: < UO1a.2 :Differentiate between RISC and CISC >: <Assessments>: <Formative>

<Mr Pramod Menase>

|  |  |  |
| --- | --- | --- |
| Set 1: Question No 1 | Set 1: Question No 2 | Set 1: Question No 3 |
| CISC includes \_\_\_\_\_\_\_\_\_complex instruction. | RISC has\_\_\_\_\_\_\_\_\_\_ performance. | The computer architecture aimed at reducing the time of execution of instructions is \_\_\_\_\_\_\_\_. |
| Recall/ Remembering | Understanding | Application |
| 1. Double | 1. Lower | 1. CISC |
| 1. Single | 1. Higher | 1. RISC |
| 1. Multi clock | 1. Medium | 1. ISA |
| 1. Tripple | 1. Moderate | 1. ANNA |
| Ans: < c > | Ans: < b > | Ans: < b > |

|  |  |  |
| --- | --- | --- |
| Set 2: Question No 1 | Set 2: Question No 2 | Set 2: Question No 3 |
| A\_\_\_\_\_\_\_\_\_\_ architecture where instructions that process data operate only on registers and are separate from instructions that access memory | \_\_\_\_\_\_\_\_emphasis on software. | Pipe-lining is a unique feature of \_\_\_\_\_\_\_. |
| Recall/ Remembering | Understanding | Application |
| 1. Read-Write | 1. RISC | 1. ISA |
| 1. load-store | 1. CISC | 1. PCI |
| 1. Up-down | 1. MISC | 1. RISC |
| 1. Right-left | 1. PISC | 1. CISC |
| Ans: < b > | Ans: < a > | Ans: < c > |